H615

HOT Cooled MWIR Module

User Expansion Component Manual

V1.0.1

Historical Versions

Version	Time	Description
V1.0.0	2024-07	Initial release
V1.0.1	2024-08	Update external sync descriptions

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1. 01-Cameralink User Expansion Component

The 01-Cameralink user expansion component includes the main interface and the Cameralink digital video interface.

1.1 Main Interface

The main interface is J30JZ/XLN15TJWA000 (J30JZPEN15ZKCAL02 recommended for pairing with the mating connector), as shown in Figure 1.1. It includes the power supply interface, RS422 serial communication interface, analog video interface, and external sync signal interface.

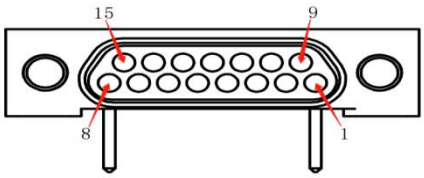

Figure 1.1 Schematic Diagram of Main Interface

The main interface is defined as shown in Table 1.1.

Table 1.1 Definition of Main Interface

Pin No.	Pin Name	Type	Description
1, 2	POWER_IN+	Power Supply	Power input (+), 12±0.5V DC
3, 4	GGND	Power GND	Power input (-), 12±0.5V DC
5	RX+_EX	Input	External sync Receive signal (+)
6	RX-_EX	Input	External sync Receive signal (-)
7	TX+_EX	Output	External sync Transmit signal (+)
8	TX-_EX	Output	External sync Transmit signal (-)
9	RS422 RX+_IR	Input	RS422 Receive signal (+)
10	RS422 RX-_IR	Input	RS422 Receive signal (-)
11	RS422 TX-_IR	Output	RS422 Transmit signal (-)
12	RS422 TX+_IR	Output	RS422 Transmit signal (+)
13	GND	Signal GND	Signal reference ground
14	VIDEO_GND	Signal GND	Analog video GND
15	VIDEO	Output	Analog Video

Note: *The signal ground cannot be used as the negative pole of DC power input.*

1.2 Description of External Sync

The module works in the set external sync mode, as shown in Table 1.2. The main interface has a group of differential external sync transmitting and receiving pins respectively, which correspond to external synchronization signal output and input modes respectively. It is suggested that the square wave shall be used as the external synchronization input signal, which shall be triggered on a rising edge by default.

Table 1.2 Description of External Synchronization

External Synchronization Mode	Module Operating Mode	Module Operating Frequency
Internal Sync (Default)	The module works normally, but it is neither controlled by the input external synchronization signal, nor outputs the external synchronization signal	50Hz
External Sync Output	The module works normally, but it is not controlled by the input external synchronization signal, and outputs the external synchronization signal	50Hz
External Sync Input	Without the external synchronization signal input, the module does not work. With the external synchronization signal input, the module is triggered for operation correspondingly	1-50Hz
Self-Adaptive	Without the external synchronization signal input, the module operates in internal sync mode. With the external synchronization signal input, the module is triggered for operation correspondingly	The working frequency is 50Hz in internal sync mode, and 1-50Hz in case of external synchronization input.

The timing of the external synchronization signal is shown in Figure 1.2 and Table 1.3.

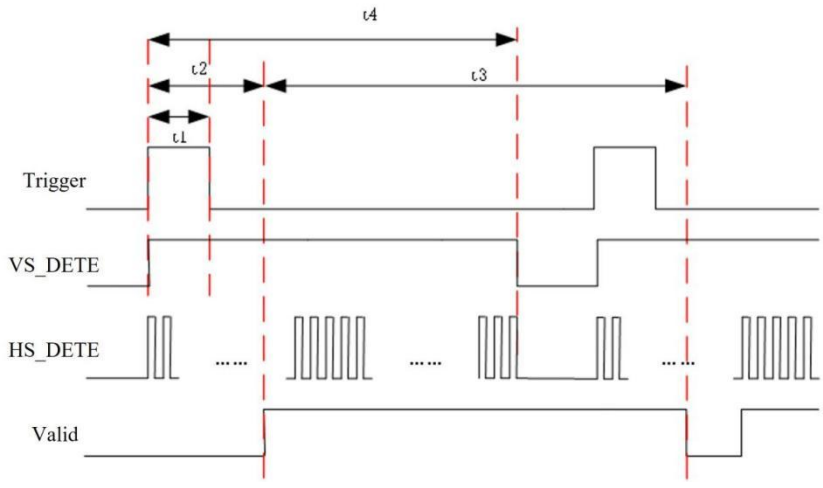

Figure 1.2 Timing of External Synchronization Signal

Note:

(1) Trigger denotes an external sync signal. VS_DETE and HS_DETE denote detector field synchronization and line synchronization signals respectively. Valid denotes a valid video output signal;

(2) t1 denotes the external synchronization signal duration, with an error of ±0.05ms;

(3) t2 denotes the initial time interval between the external synchronization signal and the valid video output signal;

(4) t3 denotes the valid output time of the video, corresponding to the time during which one frame of valid data is continuously output, with an error of ±0.05ms;

(5) t4 denotes the valid output time of the detector, corresponding to the time during which one frame of valid data is continuously output, with an error of ±0.05ms.

Table 1.3 Description of External Synchronization Signal Timing

External Synchronization-related Time	Description
t1 (external synchronization signal duration)	4ms
t2 (initial time interval between the external synchronization signal and the valid video output signal)	〈1ms
t3 (valid video output time)	11.69ms
t4 (valid detector output time)	11.70ms

1.3 Cameralink Digital Video Interface

The Cameralink digital video interface is J63A-2D2-015-221-TH (J63A-212-015-161-JC recommended for pairing with the mating connector), as shown in Figure 1.3. It includes four pairs of differential data and a pair of differential clocks.

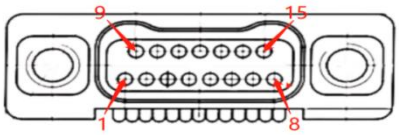

Figure 1.3 Schematic Diagram of Cameralink Digital Video Interface

The Cameralink digital video interface is defined in Table 1.4.

Table 1.4 Definition of Cameralink Digital Video Interface

Pin No.	Pin Name	Type	Description
1	CMLK-TX2-	Output	Differential data line pair #2 output negative terminal

Pin No.	Pin Name	Type	Description
2	CMLK-TX2+	Output	Differential data line pair #2 output positive terminal
3	GND	Signal GND	Signal reference ground
4	CMLK-TX1-	Output	Differential data line pair #1 output negative terminal
5	CMLK-TX1+	Output	Differential data line pair #1 output positive terminal
6	GND	Signal GND	Signal reference ground
7	CMLK-TX0-	Output	Differential data line pair #0 output negative terminal
8	CMLK-TX0+	Output	Differential data line pair #0 output positive terminal
9, 10	GND	Signal GND	Signal reference ground
11	CMLK-TXCLK-	Output	Differential clock output negative terminal
12	CMLK-TXCLK+	Output	Differential clock output positive terminal
13	GND	Signal GND	Signal reference ground
14	CMLK-TX3-	Output	Differential data line pair #3 output negative terminal
15	CMLK-TX3+	Output	Differential data line pair #3 output positive terminal

1.4 Cameralink Digital Video Timing

The module supports outputting 16- or 8-bit parallel digital video signals, including 1 clock signal (MCLK), 1 line valid signal (Hsync), 1 frame valid signal (Vsync), 16 data signals (DATA0-DATA15), and 1 data enable signal (Valid). After being processed by the Cameralink conversion chip on the user expansion component, the parallel digital video signal outputs four pairs of differential data and a pair of differential clock signals. There are 16 and 8 bits of data respectively:

When users select the original data (ORG) or non-uniformity correction (NUC) data, the data bit count is 16-bit, i.e., DATA[15:0], where DATA0 is the LSB and DATA15 is the MSB;

When users select data after image processing (DRC), the data bit count is 8-bit, i.e., DATA[7:0], where DATA0 is the LSB and DATA7 is the MSB.

The 8-bit data supports brightness/contrast adjustment, polarity switching, cross reticle control, digital zoom, image flip and other functions, which are not supported by the 16-bit data.

The Cameralink parallel digital video timing is shown in Figure 1.4. DATA recommends the rising edge sampling of MCLK. Both Hsync and Vsync are of the valid high level. Digital video outputs valid data when both Hsync and Vsync are valid.

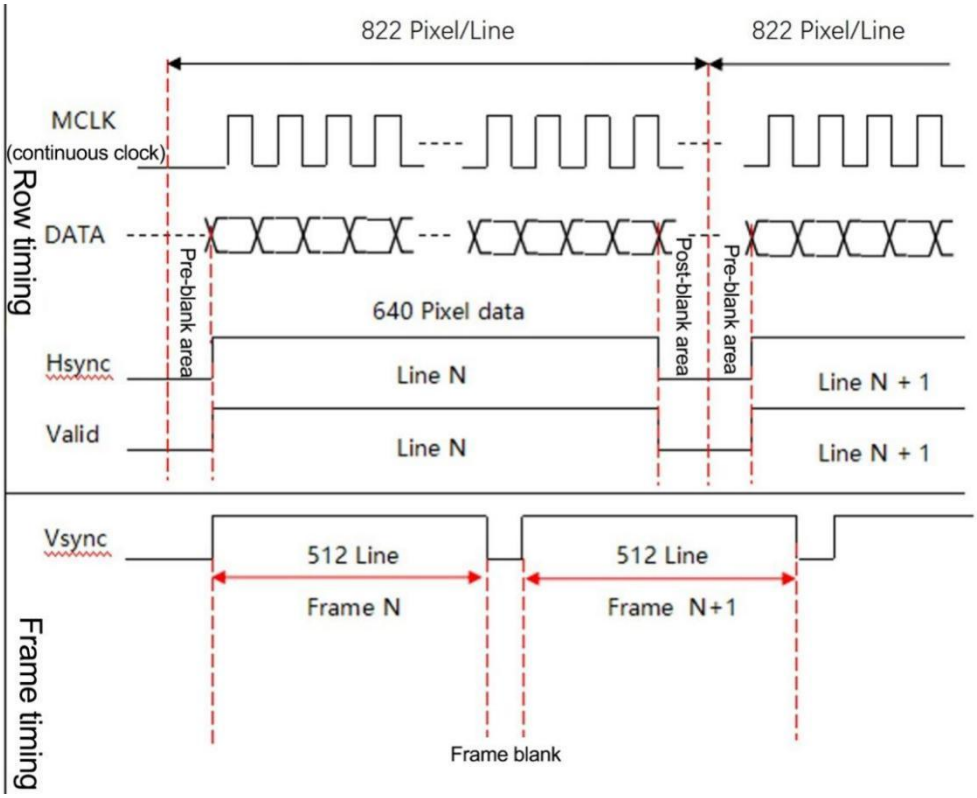

Figure 1.4 Cameralink Parallel Digital Video Timing

The Cameralink parallel digital video timing is described in Table 1.5. When Vsync is valid, both Hsync and Valid are valid for 512 times respectively, corresponding to 512 valid data lines. When Hsync and Valid are valid, they last 640 clock cycles respectively, corresponding to 640 valid pixels.

Table 1.5 Description of Cameralink Parallel Digital Video Timing

No.	Signal	Description	Remarks
1	MCLK	Clock	36MHz
2	DATA	Data	Valid data for 640 columns, 512 lines
3	Hsync	Line synchronization	Out of a total of 822 clocks, 640 clocks are high level indicating valid data, and the remaining 182 clocks are low level indicating blanking.
4	Valid	Enable	Out of a total of 822 clocks, 640 clocks are high level indicating valid data, and the remaining 182 clocks are low level indicating blanking.
5	Vsync	Frame synchronization	The 512 valid data lines indicate frame validity; and the remaining is frame-blanking lines.

2. 03-SDI User Expansion Component

The 03-SDI user expansion component includes the main interface and the SDI digital video interface.

2.1 Main Interface

The main interface is J30JZ/XLN15TJWA000 (J30JZPEN15ZKCAL02 recommended for pairing with the mating connector), as shown in Figure 2.1. It includes the power supply interface, RS422 serial communication interface, analog video interface, and external synchronization signal interface.

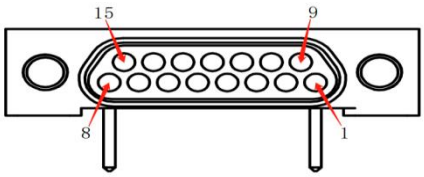

Figure 2.1 Schematic Diagram of Main Interface

The main interface is defined as shown in Table 2.1.

Table 2.1 Definition of Main Interface

Pin No.	Pin Name	Type	Description
1, 2	POWER_IN+	Power Supply	Power input (+),12±0.5V DC
3, 4	GGND	Power GND	Power input (-),12±0.5V DC
5	RX+_EX	Input	External sync Rx signal (+)
6	RX-_EX	Input	External sync Rx signal (-)
7	TX+_EX	Output	External sync Tx signal (+)
8	TX-_EX	Output	External sync Tx signal (-)
9	RS422 RX+_IR	Input	RS422 Rx signal (+)
10	RS422 RX-_IR	Input	RS422 Rx signal (-)
11	RS422 TX-_IR	Output	RS422 Tx signal (-)
12	RS422 TX+_IR	Output	RS422 Tx signal (+)
13	GND	Signal GND	Signal reference ground
14	VIDEO_GND	Signal GND	Analog video GND
15	VIDEO	Output	Analog Video

Note: *The signal ground cannot be used as the negative pole of DC power input.*

2.2 SDI Digital Video Interface

The SDI digital video interface is MMCX6252N1-3GT30G-50 (the MMCX-J male connector recommended for pairing with the mating connector), as shown in Figure 2.2.

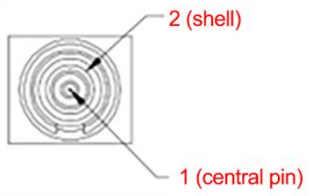

Figure 2.2 Schematic Diagram of SDI Digital Video Interface

The SDI digital video interface is defined in Table 2.2.

Table 2.2 Definition of SDI Digital Video Interface

Pin No.	Pin Name	Type	Description
1	SDI	Output	Coaxial output of SDI digital video
2	GND	Signal GND	Coaxial shell

2.3 SDI Digital Video Timing

The module supports outputting 10-bit parallel digital video signals, including 1 clock signal (CLK), 1 line valid signal (LSYNC), 1 frame valid signal (FSYNC), 10 data signals (DATA0-DATA9), and 1 data enable signal (DE). Let's take 720P@50Hz as an example. The SDI parallel digital video timing is shown in Figure 2.3.

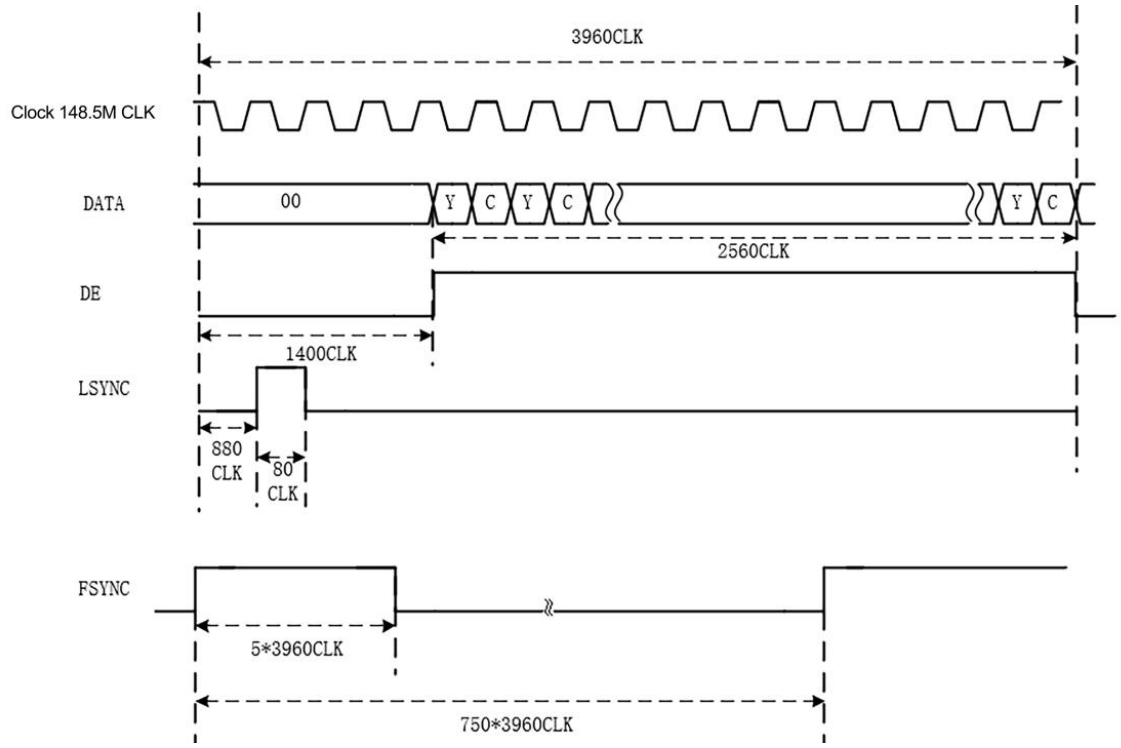

Figure 2.3 SDI Parallel Digital Video Timing

In the figure, FSYNC is at a high level for 5×3,960 clock cycles for each time, marking the start of a frame of data. LSYNC is high during clock cycles 881 to 960 within each line, indicating the start of a line of data. The 750 lines are repeated in a frame. DE is high during clock cycles 1,401 to 3,960 within each line, corresponding to 1,280 grayscale data and 1,280 chrominance data, indicating data validity. The 720 lines are repeated in a frame. CLK has a frequency of 148.5MHz.

3. Precautions

To protect yourself and others from harm or to safeguard your device from damage, please read all the following information carefully before using your device to avoid affecting your warranty rights.

1. The ideal ambient temperature is -20°C to 50°C, and the module should be powered on as per the product requirements for ambient voltage. Malfunctions caused by abnormal power-on are not covered in the warranty.
2. Do not touch the detector window with your hands or collide with them by using any objects;
3. Do not touch the module and cables with wet hands, and do not bend or damage the connecting cables.
4. Unauthorized updates to the module program are prohibited. If updates are required, please contact technical support. Unauthorized disassembly of the module is prohibited. In case of a malfunction, please contact technical support for guidance and repair. Any malfunctions caused by unauthorized repairs will not be covered by warranty.

5. Do not use chemical solvents or diluents to clean any part of the module. You can use a special lens cleaning cloth to clean the detector window. Under electrostatic protection conditions, it is allowed to use an anti-static brush or a clean, soft, dry cloth to clean the mechanical shell and circuit board surface.
6. Do not plug or unplug other cables without disconnecting the power;
7. Do not connect the provided cables incorrectly to prevent damage to the module. If the cables cannot be inserted smoothly, do not insert and remove them forcibly. Please check whether the pin is crooked, whether the insertion position is incorrect, or whether the plug is reversed.
8. Pay attention to the prevention of electrostatic discharge. When handling the module, wear an anti-static wristband and finger cots. Avoid direct contact without protection.
9. The time interval between shutting down and restarting should not be less than 10 seconds.
10. During use, adapt the integral time to the scene and perform background correction.
11. Avoid damage caused by contact with other objects during use;
12. The module should be sealed in an anti-static bag and then put into shock-absorbing sponges in the package box. When not in use, please place the module in an anti-static bag for sealed storage;
13. During storage, pay attention to protecting the module against water, moisture, impact, and drops. Damage caused by improper storage or any other natural disaster is not covered by warranty;
14. When cleaning the lens, first use a blower to blow away particles and dust. Then use degreased cotton to apply lens cleaning solution and gently wipe from the center to the edges in a single direction. Replace the cotton after each wipe. During use, minimize the frequency of wiping.